FIG. 1

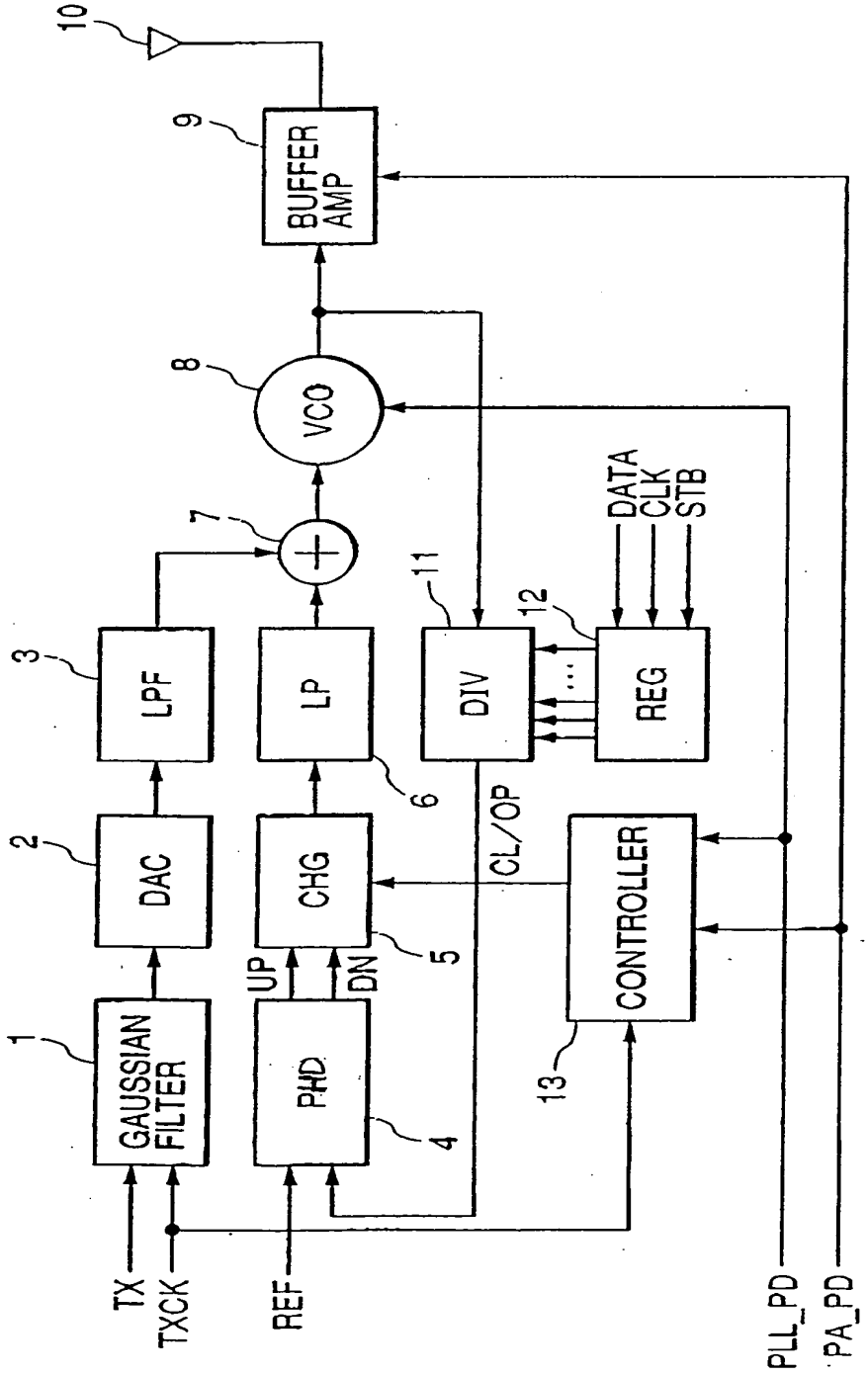

10
9
BUFFER AMP
8
VCO
7
3
LPF
LP
6
DIV
11
12
REG
DATA
CLK
STB
2
DAC
CHG
5
CL/OP
CONTROLLER
1
GAUSSIAN FILTER
UP
DN
PHD
4
13
TX
TXCK
REF
PLL_PD
PA_PD

FIG. 2

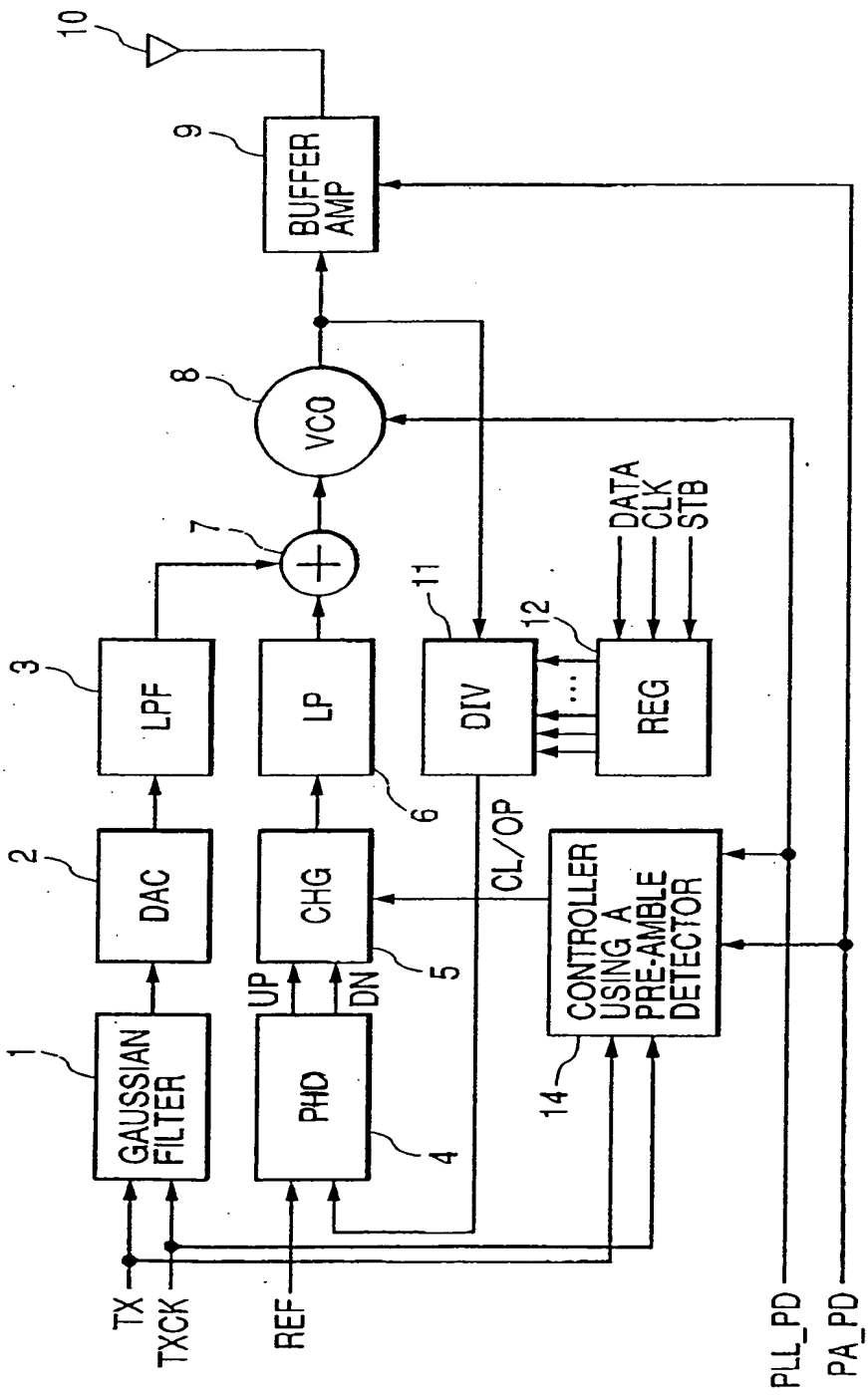

10
9
BUFFER AMP
8
VCO
7
3
LPF
LP
DIV
11
12
DATA
CLK
STB
REG
2
DAC
CHG
CL/OP
6
CONTROLLER USING A PRE-AMBLE DETECTOR
1
GAUSSIAN FILTER
UP
DN
5
PHD
4
14
TX
TXCK
REF
PLL_PD
PA_PD

FIG. 3

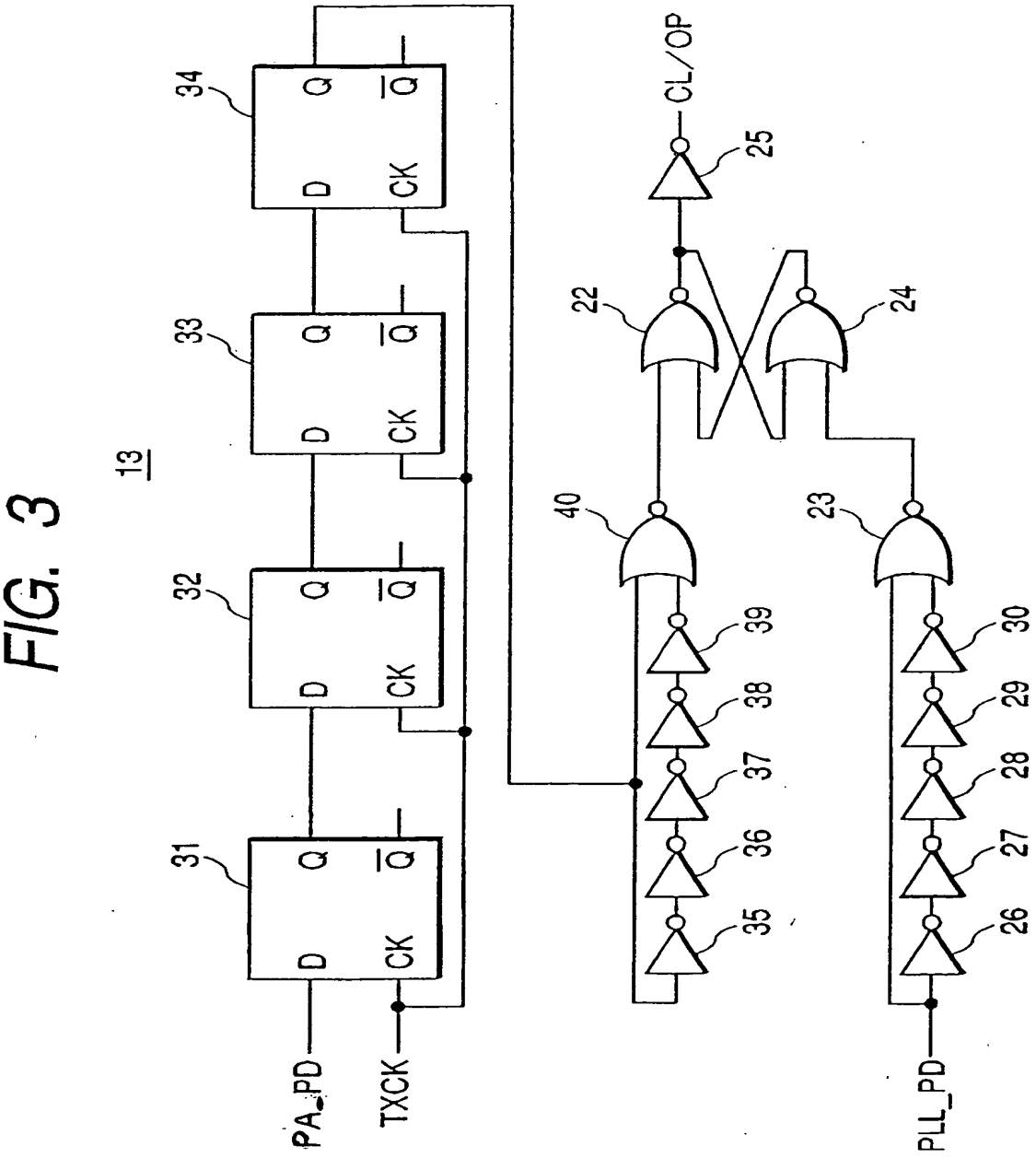

13
34
33
32
31
D
Q
CK
PA_PD
TXCK
CL/OP
25
22
24
40
23
39
38
37
36
35
30
29
28
27
26
PLL_PD

FIG. 4

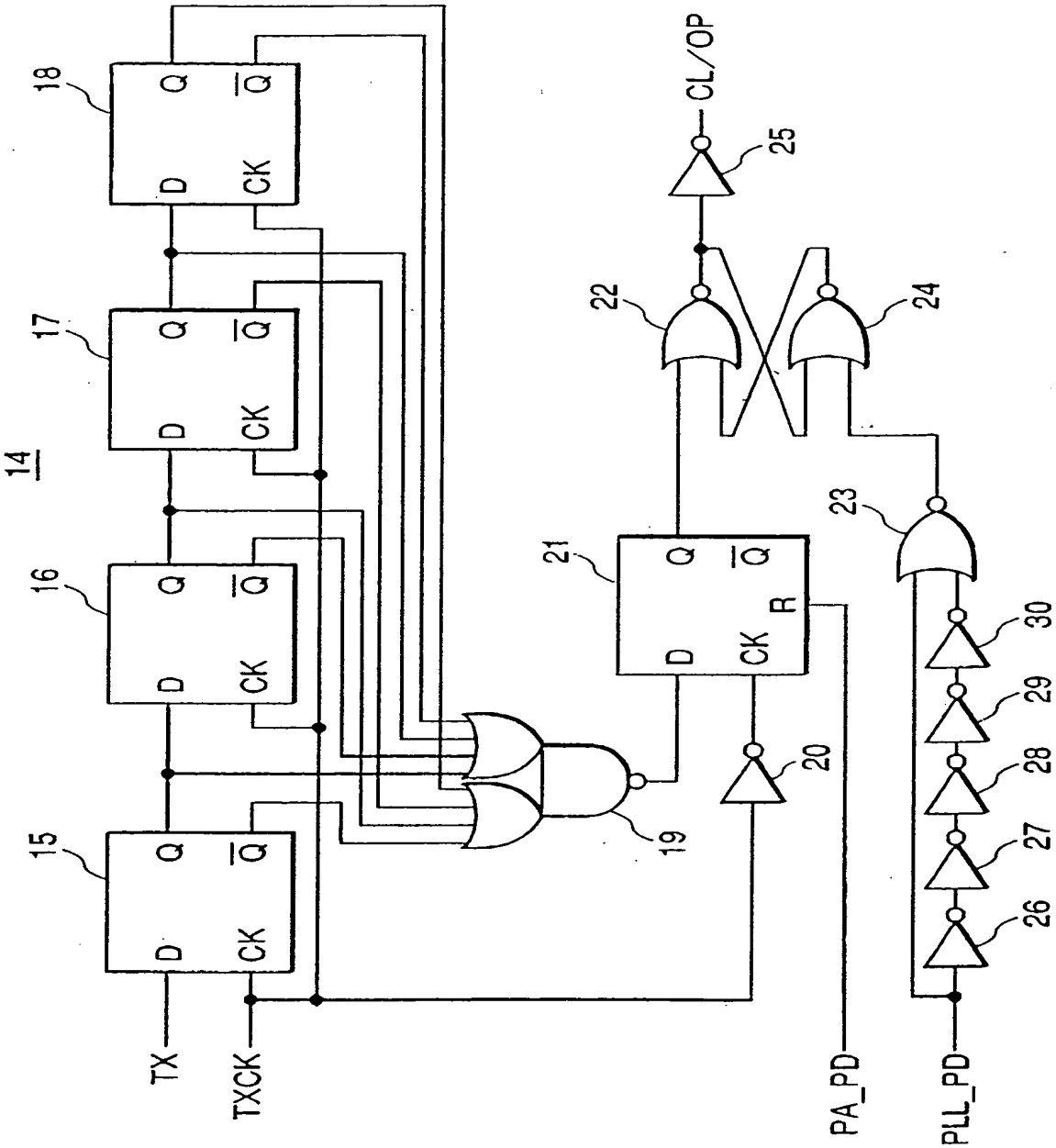

18
17
16
15
14
Q
D
CK
TX
TXCK
19
20
21
R
22
24
23
25
CL/OP
26
27
28
29
30
PA_PD
PLL_PD

FIG. 5

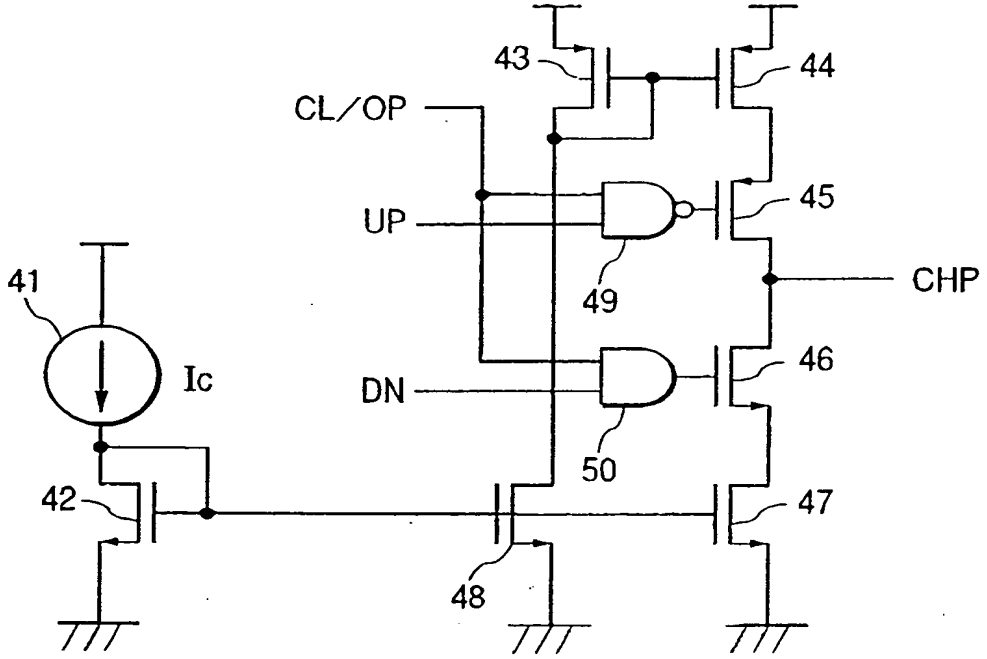
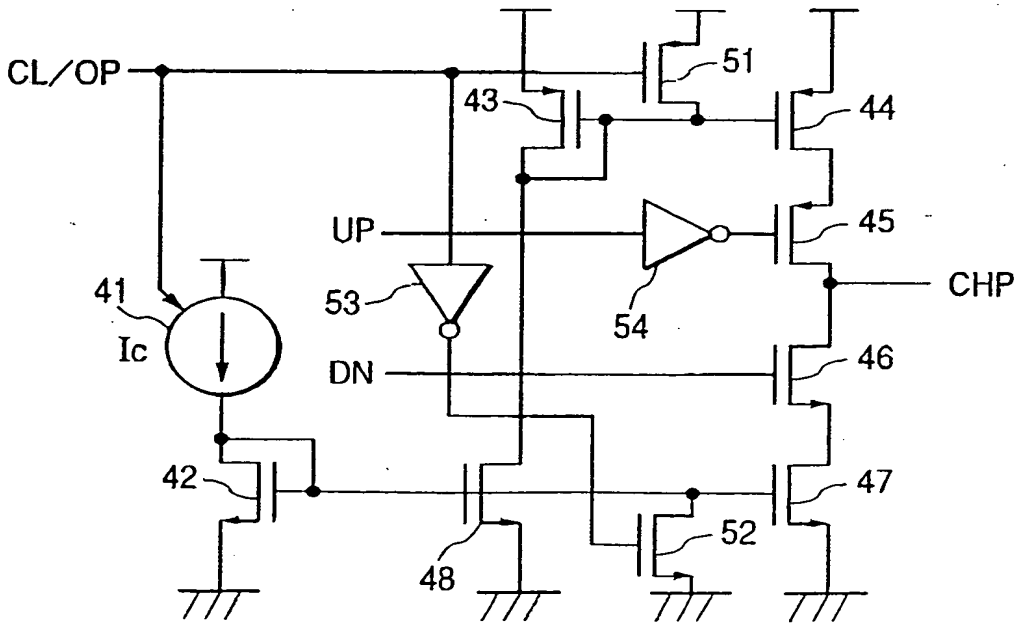


FIG. 6



EP 0 720 294 A2 960702

FIG. 7

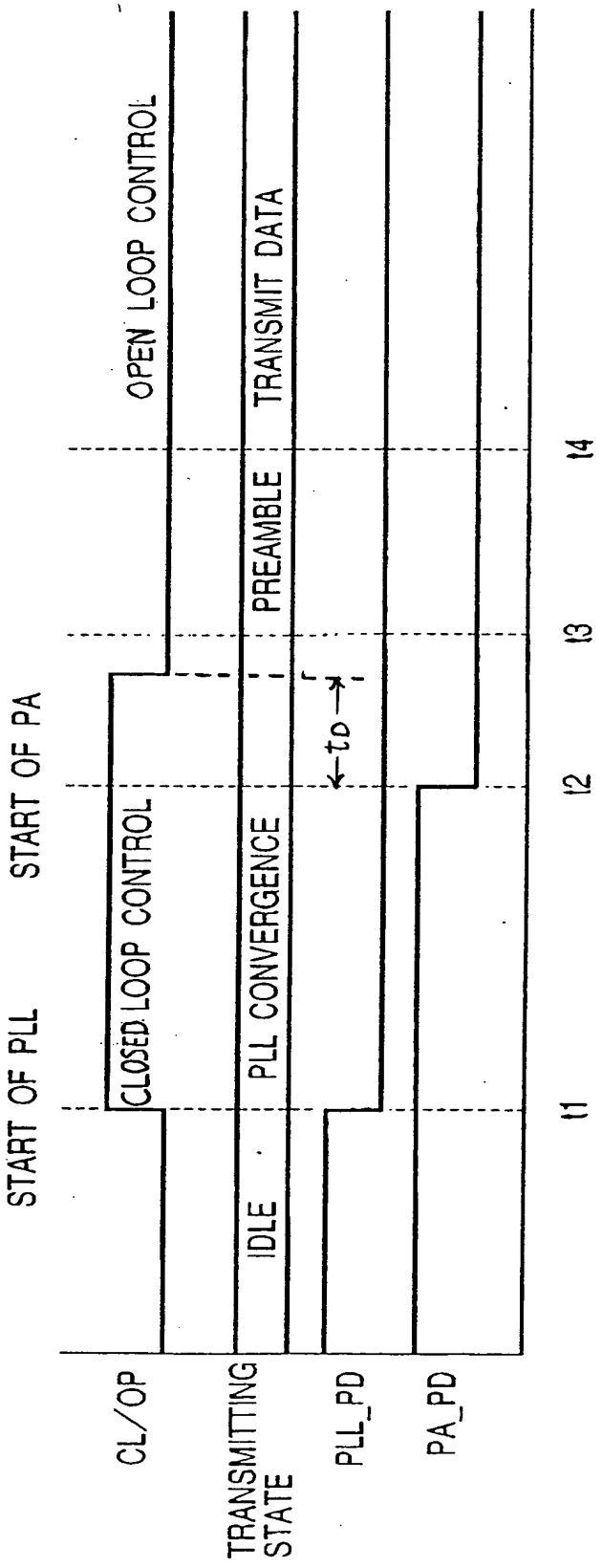

START OF PLL
START OF PA
OPEN LOOP CONTROL
CLOSED LOOP CONTROL
PLL CONVERGENCE
PREAMBLE
TRANSMIT DATA
IDLE
t_D
CL/OP
TRANSMITTING STATE
PLL_PD
PA_PD
t1
t2
t3
t4

FIG. 8

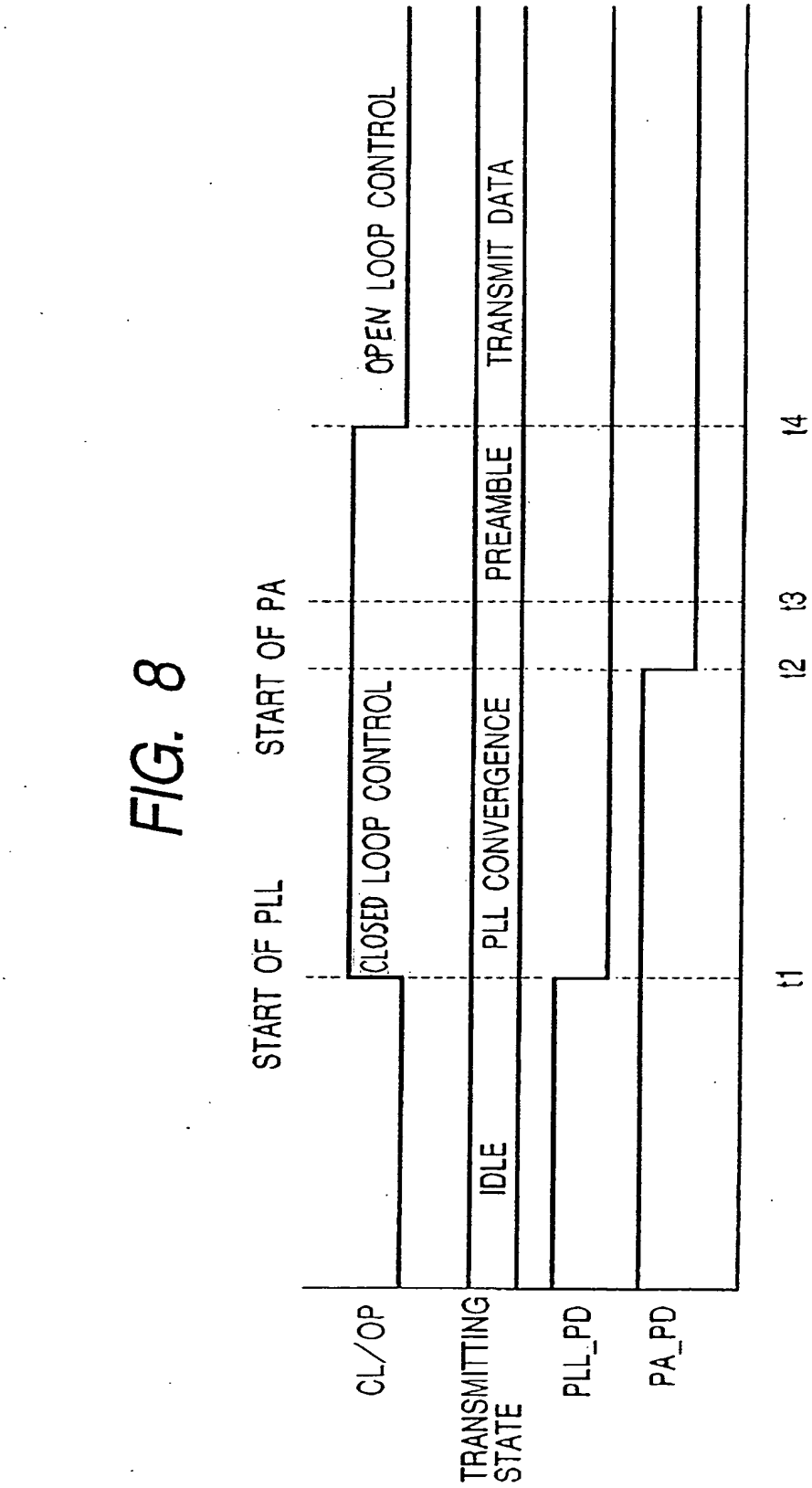

START OF PLL
START OF PA
CLOSED LOOP CONTROL
OPEN LOOP CONTROL
PLL CONVERGENCE
PREAMBLE
TRANSMIT DATA
IDLE
CL/OP
TRANSMITTING STATE
PLL_PD
PA_PD
t1
12
13
14

FIG. 9

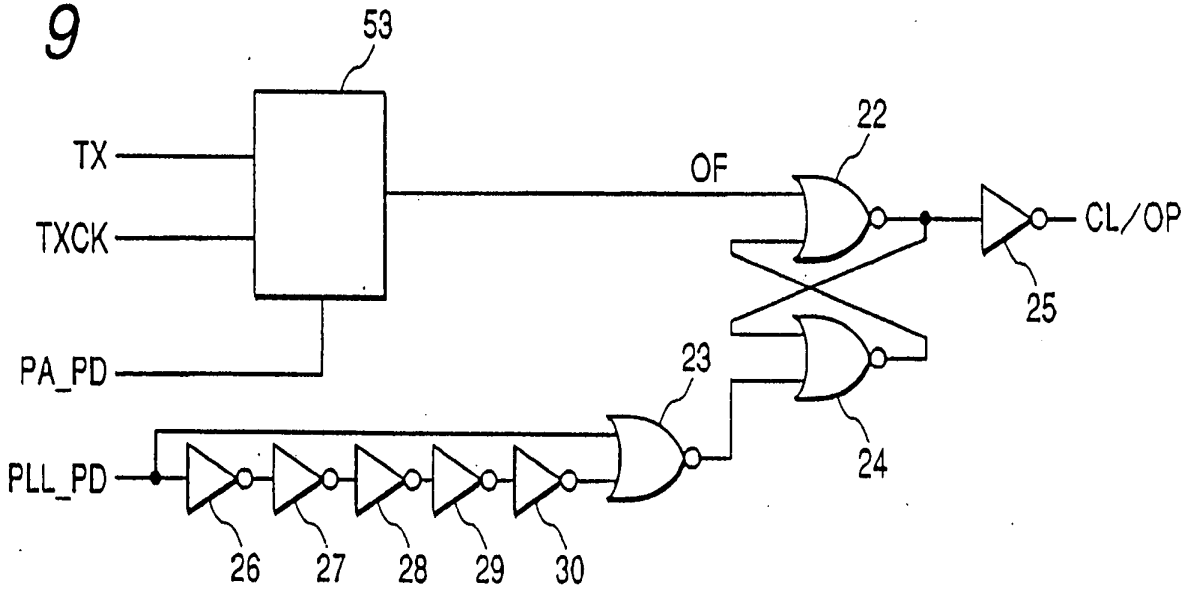
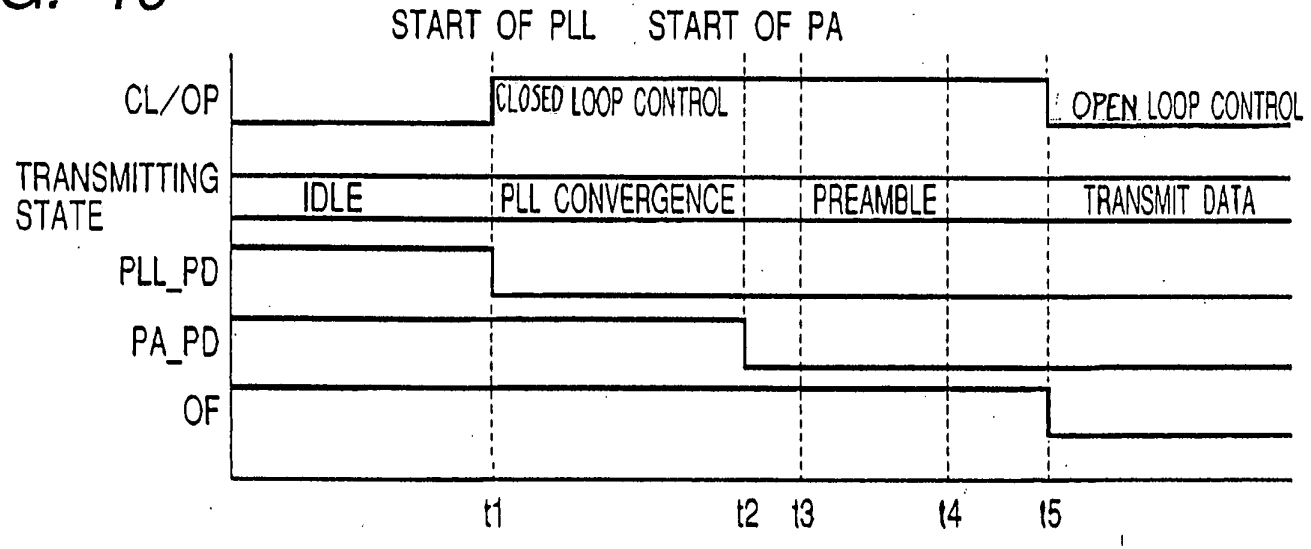

53
TX
TXCK
PA_PD
PLL_PD
OF
22
23
24
25
CL/OP
26
27
28
29
30

FIG. 10


START OF PLL
START OF PA
CL/OP
CLOSED LOOP CONTROL
OPEN LOOP CONTROL
TRANSMITTING STATE
IDLE
PLL CONVERGENCE
PREAMBLE
TRANSMIT DATA
PLL_PD
PA_PD
OF
t1
t2
t3
t4
t5

EP 0 920 129 A2

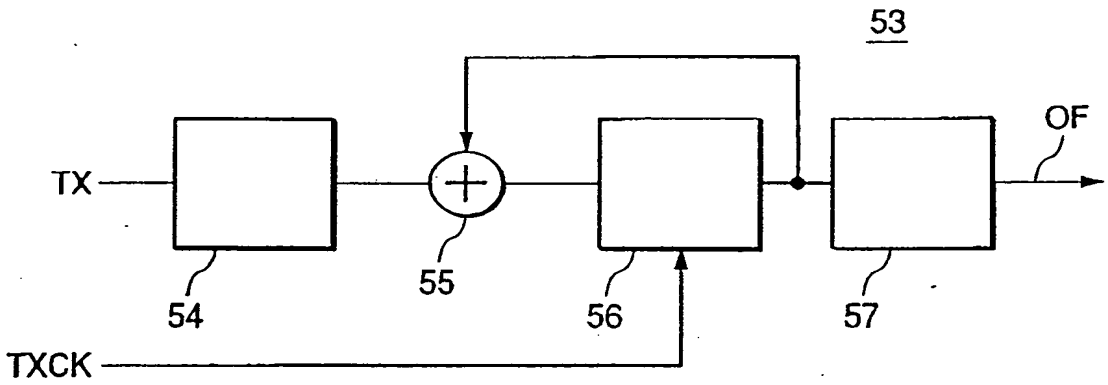



FIG. 11